

REMARKS

Claims 1-22 are pending in the application. Favorable reconsideration in light of the remarks which follow is respectfully requested.

The Obviousness Rejection

Claims 1-22 have been rejected under 35 U.S.C. § 103(a) over Mitwalsky et al (U.S. Patent 5,789,302) in view of Doerr (U.S. Patent 6,219,471). Mitwalsky et al relates to using crack stops in wafers when dicing to form individual semiconductor integrated circuit chips. The individual integrated circuit chips are in square or rectangular shape, as curvilinear cutting is NOT employed. Specifically, Mitwalsky et al forms discontinuities in the thickness of a dielectric layer near the edges of the individual integrated circuits, such as along the perimeter of the subsequently made integrated circuit chip. Doerr relates to optical devices that contain an array of optical waveguides that have straight and curved portions. Figures 3 and 4 of Doerr show "S" shaped optical waveguides, having straight and curved portions, extending between pairs of points. Doerr discusses the formation of the straight/curved waveguides.

The Examiner contends that one skilled in the art would have modified Mitwalsky et al's cutting procedure for integrated circuits by introducing curvilinear cutting as taught by Doerr. Applicants respectfully disagree for at least two reasons.

First, and most importantly, the combination of Mitwalsky et al and Doerr does not teach or suggest all of the features of the claimed invention. This is because Doerr does not disclose, teach, or suggest curvilinear cutting. While Doerr does describe curvilinear waveguides on a substrate, Doerr fails to mention dicing the substrate. This is because Doerr is only concerned with forming waveguides in a certain manner. Doerr does NOT even hint at dicing his substrate, Doerr does not hint at making curved optical integrated circuits. The curved waveguide of Doerr is not a circuit, and Doerr does not teach or suggest cutting the substrate around the curved waveguide. Moreover, Mitwalsky et al does not teach or suggest dicing optical integrated circuits. This brings us to the second deficiency in the rejection.

Second, Mitwalsky et al semiconductor integrated circuit chips, not optical integrated circuits as required by claims 1-22. This difference is notable because semiconductor integrated circuit chips are smaller than optical integrated circuits. Common semiconductor integrated circuit chips are about the size of a human thumbnail, while optical integrated circuits are several inches in length. This difference in size would motivate one skilled in the art NOT to employ curvilinear cutting on the wafer of Mitwalsky et al, because cracking would surely occur when making tight, small radial cuts in a brittle material such as silicon. That is, as the size of the chip decreases, the ability to curvilinear cut without cracking the chip also decreases. One skilled in the art would not attempt to curvilinear cut semiconductor integrated circuit chips.

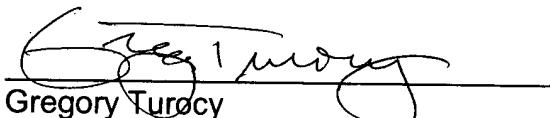
In light of the two reasons explained above, withdrawal of the rejection is respectfully requested.

Should the Examiner believe that a telephone interview would be helpful to expedite favorable prosecution, the Examiner is invited to contact Applicants' undersigned attorney at the telephone number listed below.

In the event any fees are due in connection with the filing of this document, the Commissioner is authorized to charge those fees to our Deposit Account No. 50-1063.

Respectfully submitted,

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